

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S4	1032	(determ\$5 ascertain\$3 detect\$3 assess\$3 evaluat\$3 calculat\$3) same number\$3 same (clock\$3 timer\$2) same ((differ\$3 dissimilar deviat\$3 inconsistent unequal unsimilar unlike distinct\$5) with (delay\$3))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/09 11:41
S5	241	(determ\$5 ascertain\$3 detect\$3 assess\$3 evaluat\$3 calculat\$3) with number\$3 with (clock\$3 timer\$2) same ((differ\$3 dissimilar deviat\$3 inconsistent unequal unsimilar unlike distinct\$5) with (delay\$3))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/09 11:42
S6	157	(determ\$5 ascertain\$3 detect\$3 assess\$3 evaluat\$3 calculat\$3) with number\$3 with (clock\$3 timer\$2) with ((differ\$3 dissimilar deviat\$3 inconsistent unequal unsimilar unlike distinct\$5) with (delay\$3))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/09 11:43
S7	144	((determ\$5 ascertain\$3 detect\$3 assess\$3 evaluat\$3 calculat\$3) with number\$3 with (clock\$3 timer\$2) with ((differ\$3 dissimilar deviat\$3 inconsistent unequal unsimilar unlike distinct\$5) with (delay\$3))) and @ad<"20041128"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/09 16:05
S8	2	S7 and ((determ\$5 ascertain\$3 detect\$3 assess\$3 evaluat\$3 calculat\$3) with (delay\$3 near10 (clock\$3 timer\$2)) with (pre-set (pre adj set) preset prior (in adj advance) earl\$3 (predetermin\$3 (pre adj determin\$3) (pre-determin\$3)) (pre-arrang\$3 (pre adj arrang\$3) prearrang\$3) propos\$3 beforehand) with ((constraint\$3 constrain\$4 necessit\$3 confin\$5 restrain\$4 allot\$5 allocat\$4 allow\$5 quota) near10 time\$4))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/09 11:59

S15	23	(clock with delay) and (clock with skew) and (clock near3 (allocat\$4 distribut\$5 tree)) and (clock adj2 (tree distribut\$5)) and (clock with (constrain\$4 violat\$4 budget)) and ((constraint timing delay) same clock same (met meet\$4 violat\$4 satisf\$5)) and ((optim\$6 loop\$4 iterat\$5 repeat\$4) same (skew clock timing delay) same (verif\$5 check\$4 simulat\$4 synthes\$6 violat\$5 satisf\$6)) and ((skew delay timing) same clock same (adjust\$5 add\$6 insert\$4 modif\$6)) and layout\$4 and (buffer driver) and ((timing delay skew) near3 anal\$6) and @ad<"20031128"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/13 10:17
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	Search Text
1	clock adj (Tree distribut\$4) and clock near3 skew and clock near3 delay and @ad<"20031128"
2	clock adj (Tree distribut\$4) and clock near3 skew and clock near3 delay and @ad<"20031128" and (buffer driver) same clock adj (Tree distribut\$4)
3	clock adj (Tree distribut\$4) and clock near3 skew and clock near3 delay and @ad<"20031128" and (buffer driver) same clock adj (Tree distribut\$4) and layout\$5
4	clock adj (Tree distribut\$4) and clock near3 skew and clock near3 delay and @ad<"20031128" and (buffer driver) same clock adj (Tree distribut\$4) and layout\$5 and (add\$7 insert\$5 plac\$7) with (buffer delay)
5	clock adj (Tree distribut\$4) and clock near3 skew and clock near3 delay and @ad<"20031128" and (buffer driver) same clock adj (Tree distribut\$4) and layout\$5 and (add\$7 insert\$5 plac\$7) with (buffer delay) and (verif\$6 simulat\$5 synthe\$6) with (clock skew delay)
6	clock adj (Tree distribut\$4) and clock near3 skew and clock near3 delay and @ad<"20031128" and (buffer driver) same clock adj (Tree distribut\$4) and layout\$5 and (add\$7 insert\$5 plac\$7) with (buffer delay) and (verif\$6 simulat\$5 synthe\$6) with (clock skew delay) and (optim\$8) with (clock skew delay)
7	clock adj (Tree distribut\$4) and clock near3 skew and clock near3 delay and @ad<"20031128" and (buffer driver) same clock adj (Tree distribut\$4) and layout\$5 and (add\$7 insert\$5 plac\$7) with (buffer delay) and (verif\$6 simulat\$5 synthe\$6) with (clock skew delay) and (optim\$8) with (clock skew delay) and (constrain\$4 budget slack) with (meet\$4 met violat\$4 satisf\$8)
8	clock adj (Tree distribut\$4) and clock near3 skew and clock near3 delay and @ad<"20031128" and (buffer driver) same clock adj (Tree distribut\$4) and layout\$5 and (add\$7 insert\$5 plac\$7) with (buffer delay) and (verif\$6 simulat\$5 synthe\$6) with (clock skew delay) and (optim\$8) with (clock skew delay) and (constrain\$4 budget slack) with (meet\$4 met violat\$4 satisf\$8) and (clock and delay and differ\$5)
9	clock adj (Tree distribut\$4) and clock near3 skew and clock near3 delay and @ad<"20031128" and (buffer driver) same clock adj (Tree distribut\$4) and layout\$5 and (add\$7 insert\$5 plac\$7) with (buffer delay) and (verif\$6 simulat\$5 synthe\$6) with (clock skew delay) and (optim\$8) with (clock skew delay) and (constrain\$4 budget slack) with (meet\$4 met violat\$4 satisf\$8) and (clock same delay same differ\$5)
10	clock adj (Tree distribut\$4) and clock near3 skew and clock near3 delay and @ad<"20031128" and layout\$5 and (add\$7 insert\$5 plac\$7) with (buffer driver delay) and (verif\$6 check\$5 simulat\$5 synthe\$6) with (clock skew delay) and (optim\$8) with (clock skew delay) and (constrain\$4 budget slack) with (meet\$4 met violat\$4 satisf\$8) and (clock same delay same differ\$5)
11	clock adj (Tree distribut\$4) and clock near3 skew and clock near3 delay and @ad<"20031128" and layout\$5 and (add\$7 insert\$5 plac\$7) with (buffer driver delay) and (verif\$6 check\$5 simulat\$5 synthe\$6) with (clock skew delay) and (optim\$8) with (clock skew delay) and (constrain\$4 budget slack) with (meet\$4 met violat\$4 satisf\$8) and (clock same delay same differ\$5) and (loop\$5 repeat\$4 iterat\$5) same (timing delay constrain\$4 violat\$4 satisf\$5 meet\$4 met)

	Search Text
12	clock adj (Tree distribut\$4) and clock near3 skew and clock near3 delay and @ad<"20031128" and layout\$5 and (add\$7 insert\$5 plac\$7) with (buffer driver delay) and (verif\$6 check\$5 simulat\$5 synthe\$6) with (clock skew delay) and (optim\$8) with (clock skew delay) and (constrain\$4 budget slack) with (meet\$4 met violat\$4 satisf\$8) and (clock same delay same differ\$5) and (loop\$5 repeat\$4 iterat\$5) same (timing delay constrain\$4 violat\$4 satisf\$5 meet\$4 met) and (timing delay clock) near3 (anal\$6 verif\$4 synthes\$7)
13	"6205572".pn.
14	"6205572".pn. and clock same delay same (chang\$6 adjust\$7 modif\$4 insert\$5 add\$4 plac\$5) same (layout\$4 buffer driver)
15	"6205572".pn. and (chang\$6 adjust\$7 modif\$4 insert\$5 add\$4 plac\$5) same (layout\$4 buffer driver)
16	(clock adj (Tree distribut\$4)).ab. and @ad<"20031128" and layout\$5 (buffer driver)
17	(clock adj (Tree distribut\$4)).ab. and @ad<"20031128" and layout\$5 and (buffer driver)
18	(clock adj (Tree distribut\$4)).ab. and @ad<"20031128" and layout\$5 (buffer driver) and clock same (simulat\$5 synthes\$6)
19	(clock adj (Tree distribut\$4)).ab. and @ad<"20031128" and layout\$5 and (buffer driver) and clock same (simulat\$5 synthes\$6)
20	(clock adj (Tree distribut\$4)).ab. and @ad<"20031128" and layout\$5 and (buffer driver) and clock same (simulat\$5 synthes\$6) and (loop\$5 repeat\$4 iterat\$5) same (timing delay constrain\$4 violat\$4 satisf\$5 meet\$4 met) and (timing delay clock) near3 (anal\$6 verif\$4 synthes\$7) and clock near3 skew
21	(clock adj (Tree distribut\$4)).ab. and @ad<"20031128" and layout\$5 and (buffer driver) and clock same (simulat\$5 synthes\$6) and (loop\$5 repeat\$4 iterat\$5) same (timing delay constrain\$4 violat\$4 satisf\$5 meet\$4 met) and (timing delay clock) near3 (anal\$6 verif\$4 synthes\$7) and clock near3 skew and optim\$7 same clock same (timing delay skew slack)